

REMARKS

Examiner Maria F. Guerrero is thanked for thoroughly reviewing the instant application and for examining the Prior Art.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested. Claims 13-24 are pending.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 13-24 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,180,501) in view of Bartush (U.S. Patent 5,365,866) is respectfully requested based on the following.

Pey et al. provides for the creation of a double polysilicon gate structure, the instant claimed invention provides for a method of fabricating field effect transistors having low sheet resistance gate electrodes.

Specifically, Pey et al. provides for:

- Fig. 4, a gate electrode having a silicon nitride cap 22 and silicon nitride gate spacers 20
- Fig. 6, a layer 26 of Ti/TiN is deposited for purposes of salicidation
- Fig. 8, after salicidation (Fig. 7) a layer 32 of TEOS is deposited and polished (Fig. 9)
- Fig. 10, and contact opening 36 is created in the layer of TEOS for access to the top of gate electrode
- Figs. 11 through 12c, a second poly gate is formed as an extension of the first poly gate 12 (40, a stud shaped additional gate in Fig. 12a; 42, a T-shaped additional gate in Fig. 12b; and 43, a relatively short stud shaped additional gate in Fig. 12c); these extended gate electrodes are shown in Fig. 13a (the extended stud shape) and 13b (the T-shaped) after layer 44 of photoresist has been removed from the surface
- Fig. 13c through 15b, a thin layer 46 of Ti/Tin or Cobalt/Titanium is deposited and salicided over the extended gate structure, forming salicided layer 48, in Fig. 15a for the stud shaped extended gate structure, in Fig. 15b for the T-shaped extended gate structure and in Fig. 14c for the relatively short stud shaped extended gate structure.

The instant claimed invention provides for, essentially following claim 13 of the instant claimed invention:

- Figs. 8-9, providing a gate structure with salicided source/drain contact surfaces over a semiconductor substrate, a layer 17 of BN is the top layer of the gate electrode
- Fig. 9, depositing a liner layer 31 of silicon dioxide
- Fig. 9, depositing a layer 33 of photoresist over the liner layer 31
- Fig. 10, polishing the surface of the layer of photoresist down to the surface of the layer 17 of BN, using the layer 17 of BN as a stop for the process of polishing
- Fig. 11, removing the layer 17 of BN from above the one gate electrode, exposing the surface of the gate electrode
- Fig. 12, depositing a thick layer 35 of Ti/TiN as salicide material over the surface of the polished layer of dielectric including the exposed surface of the gate electrode
- Fig. 12 applying a low temperature anneal, annealing the deposited thick layer 35 of salicide material, saliciding the top surface of the gate electrode
- Fig. 13, applying a selective etch to remove un-salicided material, and
- Fig. 13, performing a high temperature anneal.

The difference between the instant claimed invention and the invention provided by Pey et al. can best be illustrated by highlighting the steps that are provided by Pey et al. that are not part of the instant claimed invention, as follows.

The instant claimed invention does not provide the following steps that are provided by Pey et al.:

- providing a gate electrode having a silicon nitride cap 10 (not highlighted but initially highlighted as layer 10, Fig. 1 of Pet et al.) and silicon nitride gate spacers 20
- depositing a layer 32 of TEOS (Fig. 8, Pet et al.), the TEOS is polished (Fig. 9, Pet et al.)
- creating a contact opening 36, Fig. 10 Pet et al., through a layer 34 of TEOS for access to the top of gate electrode; the top layer 22 if nitride is removed from the surface of the gate electrode, exposing the layer 12 of polysilicon
- depositing a layer 38, Fig. 11 of Pet et al., of polysilicon for the formation of extended gate electrodes
- patterning and etching the deposited layer 38, fig. 11 pf Pet et al., of polysilicon, forming a (extended plug shaped or T-shaped or relatively short stud shaped) second poly gate as an extension of the first poly gate
- saliciding the surface of the second poly gate.

Inversely, the instant claimed invention provides for the following steps that are not provided by Pey et al.:

- providing the gate electrode with a top layer of BN
- depositing a layer of liner oxide over a gate electrode that has been provided with salicided source/drain surfaces
- depositing a layer of dielectric, preferably comprising photoresist, over the surface of the layer of etch stop material
- polishing the surface of the layer of dielectric down to the surface of the layer of BN, using the layer of BN as a stop for the process of polishing
- removing the layer of BN material from above the one gate electrode
- depositing a thick layer of Ti/TiN over the surface of the polished layer of dielectric including the exposed surface of the gate electrode
- performing a low temperature anneal, annealing the deposited thick layer of salicide material, saliciding the top surface of the gate electrode
- selectively removing un-reacted Ti/Tin, and
- performing a low temperature anneal.

Bartush provides for the creation of a gate electrode over a substrate whereby the sequence provided by Bartush is

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significantly different from the processing sequence that is provided by the instant claimed invention. More specifically:

- Bartush provides a stack of patterned layers comprising a layer 12 of polysilicon over which a layer 14 of insulation (Ni/O₂) over which a layer 16 of boron nitride
- oxidized sidewalls 12' are formed
- as part of the formation of the oxidized sidewalls, the layer 16 of boron nitride is also oxidized, forming the oxidized boron nitride layer 16'
- layer 16', see col. 4, lines 1 e a., is now substantially free of boron; the boron in the original nitride layer 16 reacts with oxygen during the rapid thermal oxidation process to form boric acid; since boric acid is volatile at the pressure and temperature that are applied for the formation of sidewalls 12', the boric acid vaporizes
- a barrier layer 20 is deposited
- a layer 22 of insulation material is deposited
- the layer 22 of insulation material is polished, removing at the same time the barrier layer from the surface of the oxidized boron nitride layer 16'; this polish applied CMP and does use the oxidized boron nitride layer 16' as a stop layer, and
- the process then continues with deposition of a mandrel extension layer 24 of for instance oxide.

From the above it can be concluded that the CMP polish stop layer that is used by Bartush is an oxidized boron nitride layer, the instant claimed invention uses a layer of boron nitride for this purpose.

It is respectfully submitted by Applicant that commonality of one step between Bartush and the instant claimed invention does not negate the unique nature of the instant claimed invention, as can be further confirmed by referring to claim 13 of the instant claimed invention, which provides for fabricating of field effect transistors having low sheet resistance gate electrodes. Underlined in this claim are those aspects of the instant claimed invention that are not provided by Bartush. Claim 13 is following quoted in its totality to further demonstrate that the instant claimed invention provides for a complete and comprehensive method of creating field effect transistors having low sheet resistance gate electrodes, as follows:

- providing a semiconductor substrate, the substrate having been provided with at least one gate electrode created over an active surface region as the substrate as defined by regions of Shallow Trench Isolation provided in the surface of the substrate, the at least one gate electrode having been provided with gate spacers, impurity implants of source and

drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of the substrate self-aligned with the at least one gate electrode, the at least one gate electrode comprising a stack of layers of pad oxide created over the surface of the substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon

- depositing a thin layer of salicide material over the surface of the substrate, including the surface of the gate spacers and the layer of polysilicon provided for the at least one gate electrode
- performing a first anneal, forming salicided layers comprising reacted salicide material over the surface of the source and drain implants
- first removing un-reacted salicide material from the surface of the substrate
- depositing an isolation film over the surface of the substrate, including the surface of the gate spacers and the layer of boronitride provided for the at least one gate electrode
- depositing a layer of filler material over the surface of the isolation film to a thickness such that the surface of the layer of filler material extends above the surface of the

isolation film even where the isolation film overlays the surface of the at least one gate electrode

- polishing the surface of the layer of filler material and the layer of isolation film down to the surface of the layer of boronitride of the at least one gate electrode, using the layer of boronitride as a stop for the process of polishing, advantageously using a polishing rate of filler material that is larger than a polishing rate of boronitride, the layer of boronitride providing a save stop for the polishing the surface of the layer of filler material and the layer of isolation film, thereby further preventing corrosion of the surface of the at least one gate electrode
- removing the layer of boronitride from the at least one gate electrode, exposing the surface of the layer of polysilicon forming part of the at least one gate electrode
- depositing a thick layer of salicide material over the surface of the polished layer of filler material, including the exposed surface of the layer of polysilicon
- performing a second anneal of the deposited thick layer of salicide material, a layer of reacted salicide material overlying the layer of polysilicon of the at least one gate electrode

- second removing un-reacted salicide material from the surface of the layer of dielectric, and
- performing a third anneal, reducing the sheet resistance of the reacted salicide material overlying the layer of polysilicon of the at least one gate electrode.

As has been stated supra, the CMP polish stop layer that is used by the instant claimed invention comprises boronitride, the layer that is used by Bartush comprises oxidized boron nitride. It is respectfully suggested that the (Bartush) layer of oxidized boron nitride has an polishing selectivity that differs from the polishing selectivity of a layer of boron nitride since the oxidation of the layer of boron nitride, which takes place in the Bartush invention, changes the molecular structure of the layer of boron nitride. It is therefore to be expected that, in addition to the above highlighted comprehensive aspects of the instant claimed invention, the polishing process that is provided by the instant claimed invention differs from the polishing process that is provided by Bartush, this in light of the observation that both inventions use a layer of specific polishing selectivity as a polishing stop layer.

The differences between the instant claimed invention and the claimed invention provided by Bartush can be summarized by

stating that the latter invention provides a layer of oxidized boron nitride as a stop layer for Chemical Mechanical Polishing while the instant claimed invention provides a complete processing sequence for forming field effect transistors having low sheet resistance gate electrodes. One of the steps that is used by the instant claimed invention in this complete processing cycle is the use of a layer of boron nitride as a stop layer for Chemical Mechanical Polishing.

This however does not make the instant claimed invention obvious based on the Bartush invention. If for instance and to demonstrate the latter point, two different inventions commonly share a step of temperature cycling (up-ramping and down-ramping of a temperature as a function of time) then it cannot reasonably be suggested that these two inventions are identical based on this one commonality. A significant number of other steps of the two inventions are different, just like a significant number of steps of the instant claimed invention differ from the steps provided by Bartush, as has been highlighted in detail above, while the instant claimed invention provides processing steps that are not provided by Bartush.

The advantages that are provided by key aspects of the instant claimed invention are that, since the polishing

selectivity for photoresist (layer 33, Fig. 9) and silicon oxide (PR/SiO₂, layer 31, Fig. 9) is larger than about 30 and the polishing selectivity for photoresist/BN (PR/BN) is larger than about 200, the polishing process of the instant claimed invention can safely stop on the layer 17 of BN, in this manner preventing the typical corrosion of a conventional process.

It is not known how these polishing characteristics and the polishing stop capability of a layer of oxidized boron nitride compare with the above quoted polishing characteristics of the Bartush invention.

While applicant acknowledges the teachings of Pey et al. and Bartush as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Pey et al. with Bartush, applicant nonetheless also asserts that there is absent within the portions of Pey et al. and Bartush or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's claimed invention as taught and claimed within amended claim 13.

In this regard, applicant claims that there is absent from the portions of Pey et al. and Bartush or any combination thereof, as cited by Examiner, a teaching of enabling accessing the top surface of the layer of polysilicon that is used for the gate electrode for purposes of saliciding this layer. By providing a layer of boron nitride over the surface of the layer of polysilicon, this layer allows the effective separation of first saliciding the source/drain regions of the gate electrode (Fig. 9 of the instant claimed invention) and then and as a separate processing sequence (Figs. 10-13 of the instant claimed invention) saliciding the surface of the gate electrode. For this latter salicidation, surfaces that are not to salicided, that is all surfaces other than the surface of the layer of polysilicon of the gate electrode, must be protected, a protection that is provided by layer 31 of silicon oxide and layer 33 of filler (photoresist) material. The layer 17 of boron nitride is critically important in the removal, down to the surface of the layer 17 of boron nitride, of the layer of filler (photoresist) material, a removal that is most readily affected by applying CMP to the layer of filler material. For this CMP a good end-point must be provided for obvious reasons of closeness of elements (gate spacers, gate electrode material). This good end point is provided by the layer of boron nitride. After the layer of filler material has been polished, the layer of boron

nitride must be removed so that the layer of polysilicon is exposed and can be salicided as a separate processing sequence (Figs. 12, 13 of the instant claimed invention).

It would not be obvious to combine the teachings of Pey et al. with those of Bartush since there is no suggestion or motivation in the teachings of any of the patents of the present claimed invention. Contrary to the Examiner's assertion that Pey et al. provides for a gate electrode that would suggest the process of the instant claimed invention, Pey et al. does not provide for a cost-effective and dependable method of first saliciding the source/drain surfaces and then saliciding the gate electrode. Pey et al. discloses forming a double-polysilicon gate structure and does not mention the formation of a single-polysilicon gate electrode with separate processing sequences for the salicidation of the source/drain surfaces and the surface of the gate electrode.

None of the applied or known references address the claimed invention as shown in the amended claims in which a gate electrode is created, the contact surfaces of the gate electrode are salicided as separate processing step and a method is provided for the protection of the layer of gate material up to the point where this surface is salicided, thereby assuring a

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low contact resistance surface of the gate electrode. The claimed invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own claimed invention. None of the applied references address the problem of gate electrode salicidation as provided by the instant claimed invention and as specified in amended claim 13 and supporting claims of the instant claimed invention. The processes of Figs. 8-13 (Claims 13-24) are both believed to be novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request Examiner Maria F. Guerrero to reconsider his rejection in view of these arguments and the amendments to the Claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 13-24 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent

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6,180,501) in view of Bartush (U.S. Patent 5,365,866), be
withdrawn.

Other Considerations

No new independent or dependent claims have been written as
a result of this office action, no new charges are therefore
incurred due to this office action.

It is requested that should Examiner not find the claims to
be allowable that he call the undersigned Attorney at his
convenience at 845-452-5863 to overcome any problems preventing
allowance.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'S. B. Ackerman', written over the printed name.

Stephen B. Ackerman (Reg. No 37,761)